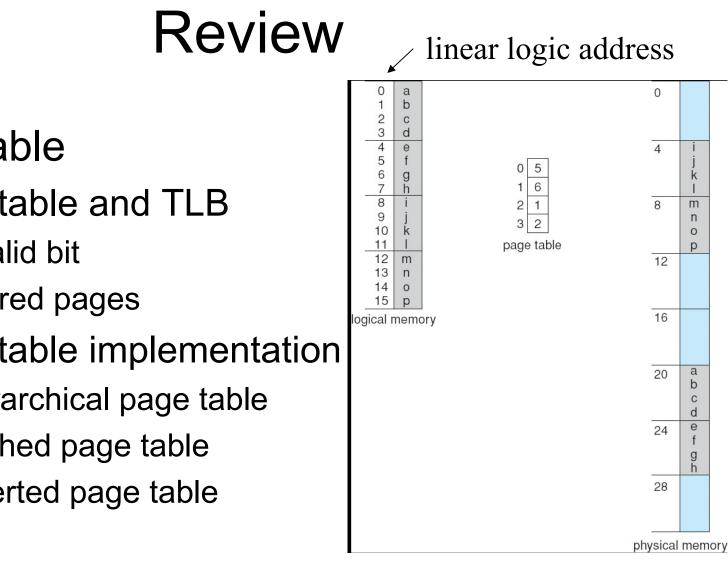
CSc 360 Operating Systems Segmentation

> Jianping Pan Summer 2015

> > 1

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- Page table
 - page table and TLB
 - invalid bit
 - shared pages
 - page table implementation
 - hierarchical page table
 - hashed page table
 - inverted page table

What's next?

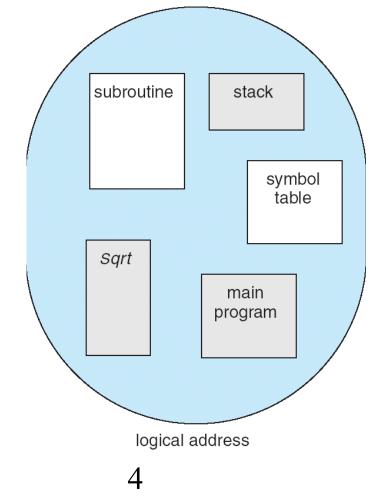
- Today's topics
 - segmentation and paging
 - examples in Intel Pentium and Linux

User's view of a program

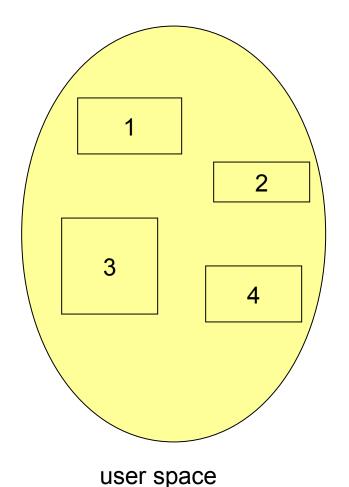
- A collection of segments
 - main program
 - symbol table
 - procedures/functions

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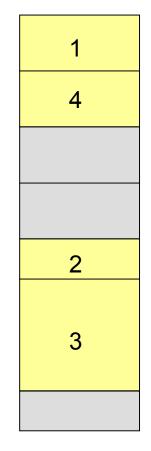
- data
- stacks
- heaps



Logical view of segmentation



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physical memory space 5

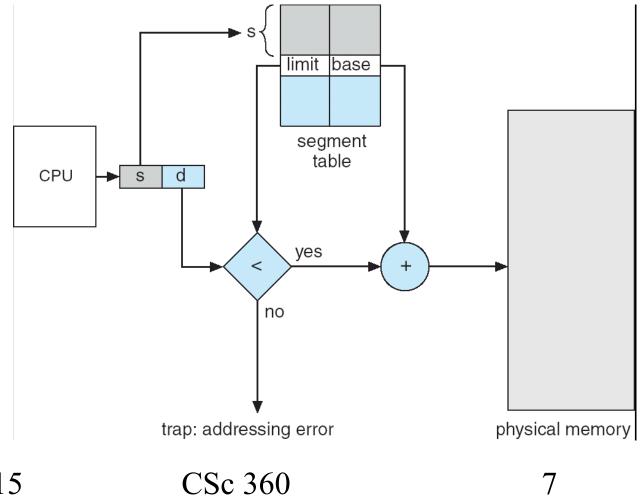
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Segmentation Architecture

- Logical address consists of a two tuple: <segment-number, offset>,
- Segment table maps two-dimensional physical addresses; each table entry has:
 - base contains the starting physical address where the segments reside in memory
 - limit specifies the length of the segment
- Segment-table base register (STBR) points to the segment table's location in memory
- Segment-table length register (STLR) indicates number of segments used by a program;

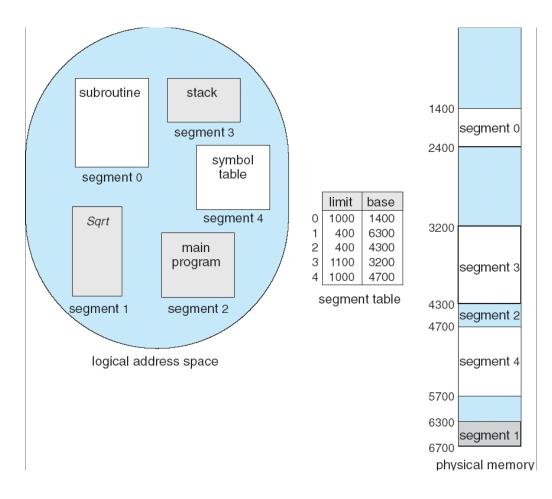
segment number s is legal if s < STLR</th>6/25/15CSc 3606

Segment table



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Example of segmenting

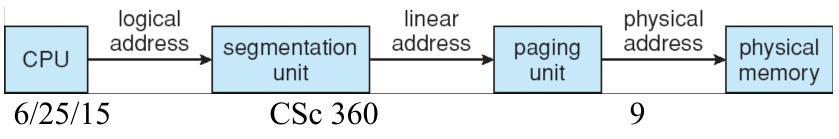


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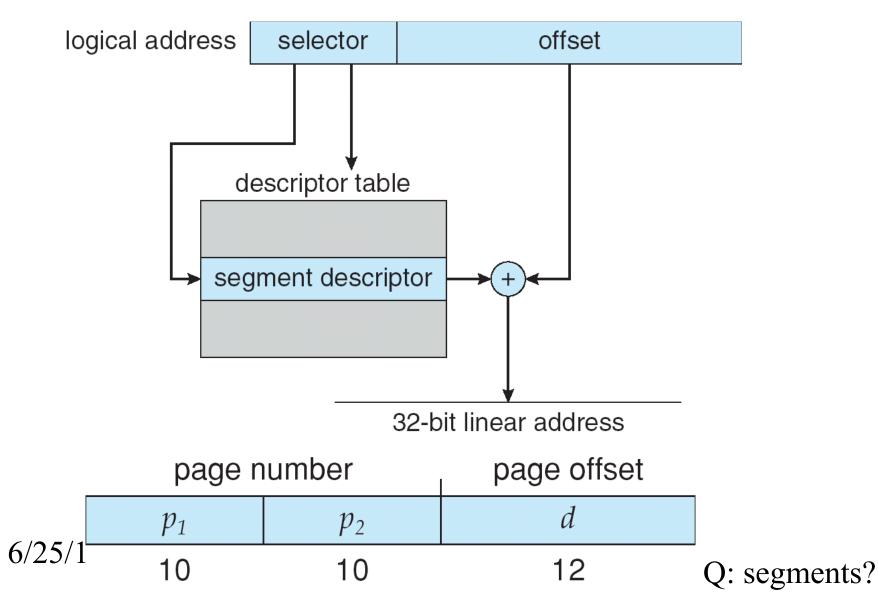
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Examples: Intel Pentium

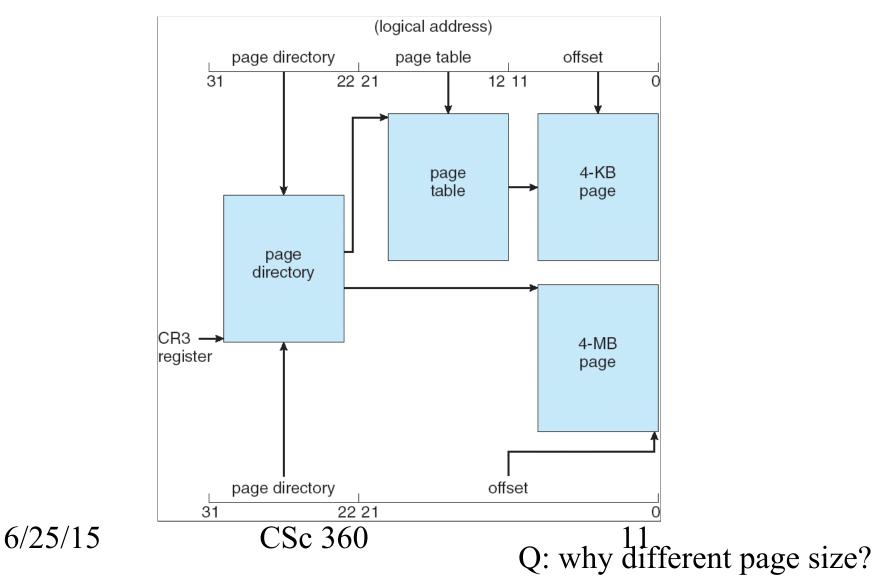
- Supports both segmentation and segmentation with paging
- -CPU generates logical address
 - Given to segmentation unit
 - Which produces linear addresses
 - Linear address given to paging unit
 - Which generates physical address in main memory
 - Paging units form equivalent of MMU



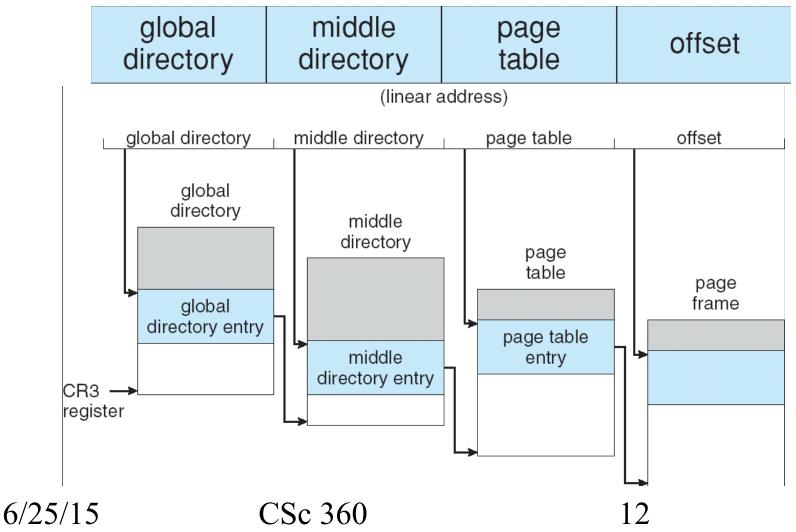
From logical to physical address



From logical to physical II



Examples: Linux paging



This lecture

- Segmentation and paging
 - user/program's view
 - segment table
 - examples
 - Intel Pentium
 - Linux

Next lecture

- Virtual memory
 - what if the main memory is not enough?
 read OSC7Ch9