CSc 360
Operating Systems
Page Table

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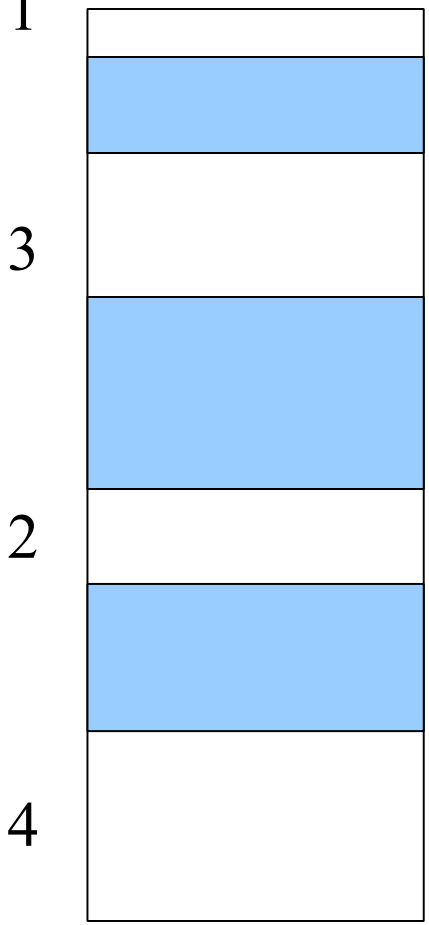
Summer

Review

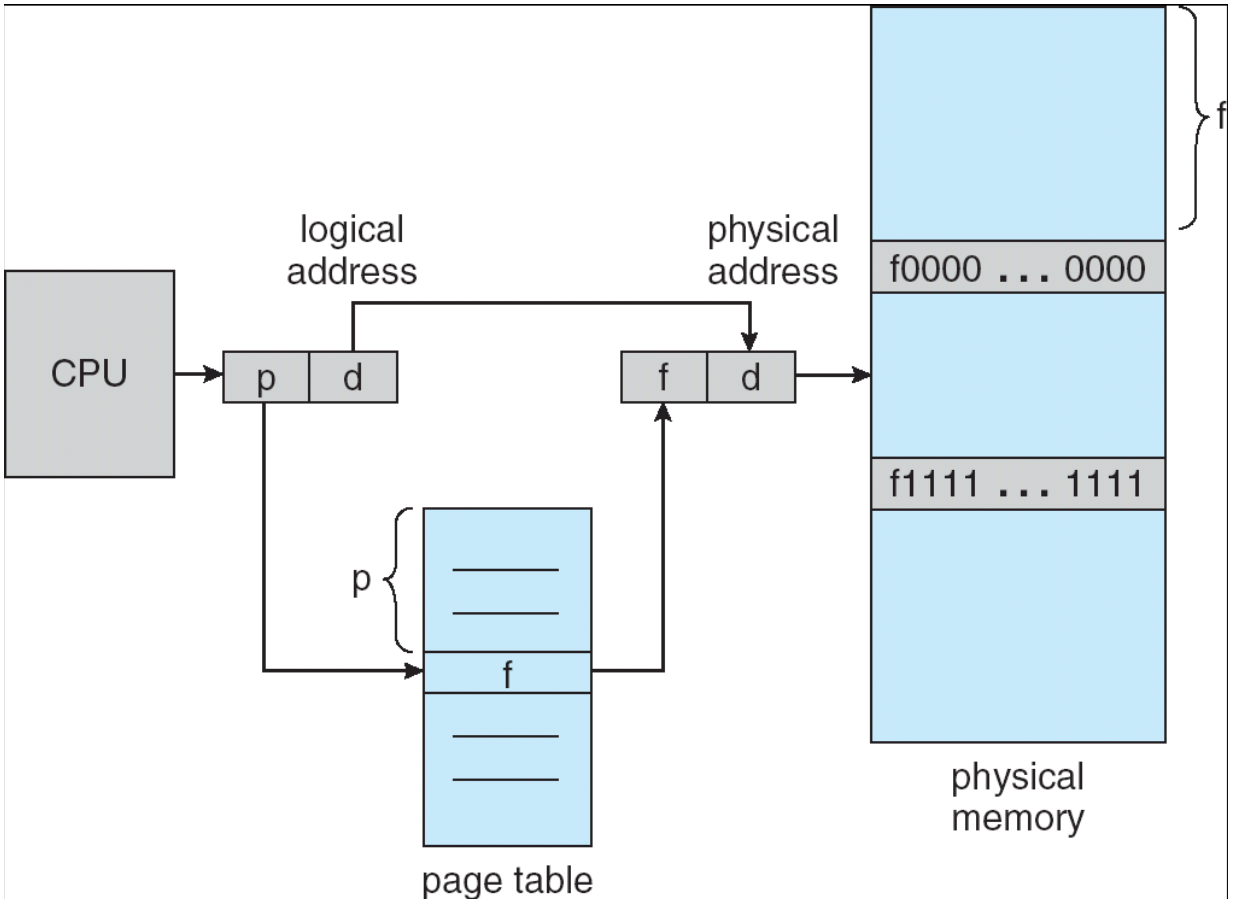
- Memory allocation
  - partition
    - first/last fit
    - best/worst fit
  - fragmentation
    - external vs internal
  - paging
    - page size: usually 0.5 to 8 KB
    - page table: mapping page# to frame#



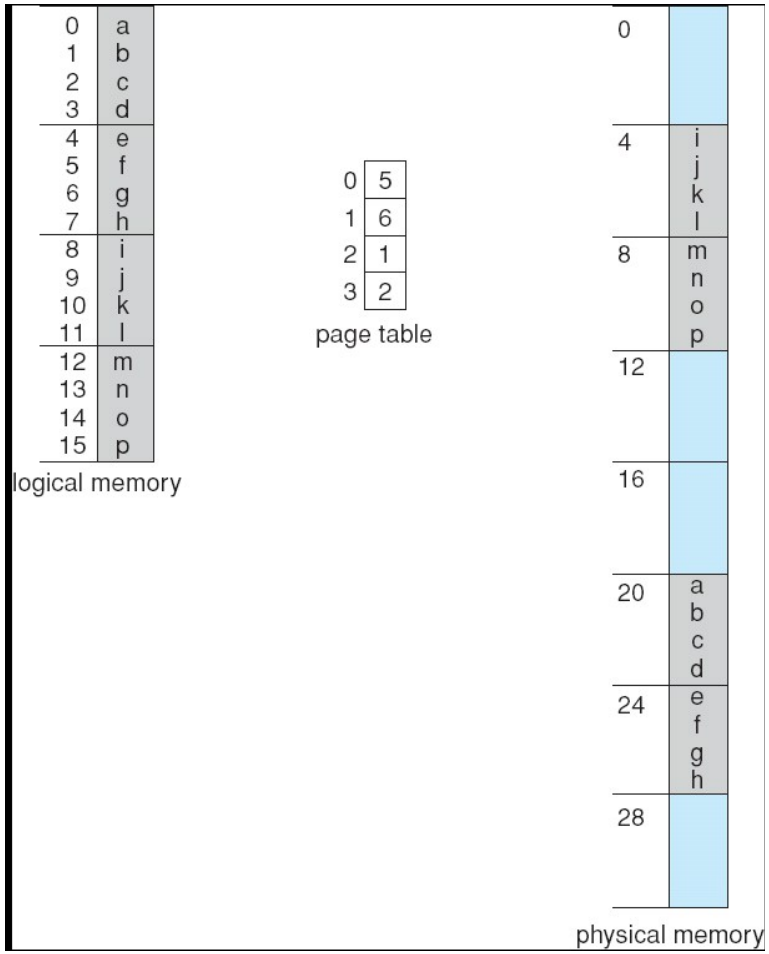
What's next?

- Today's topics
  - page table design and implementation
  - practical issues

Page table

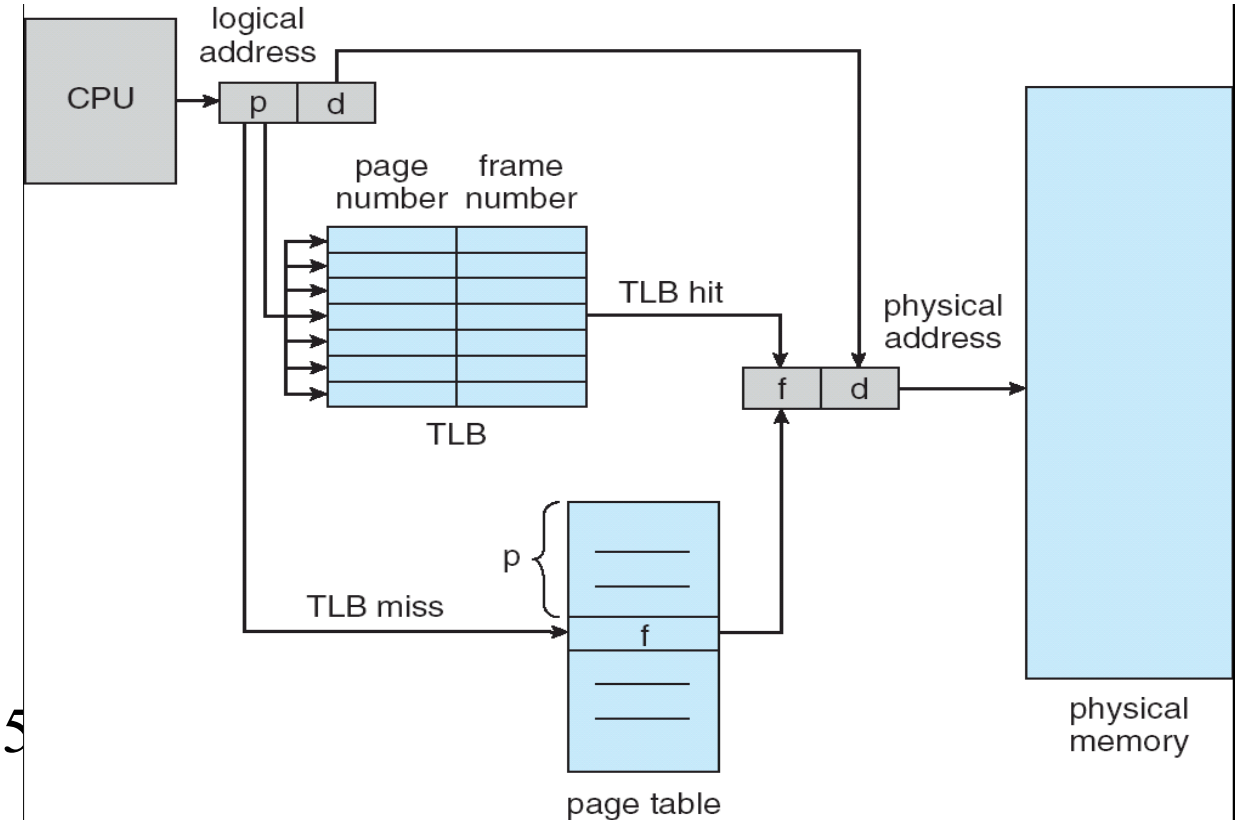

CPU
logical address
p
d
physical address
f
d
f0000 . . . 0000
f1111 . . . 1111
f
p
f
page table
physical memory

Paging example

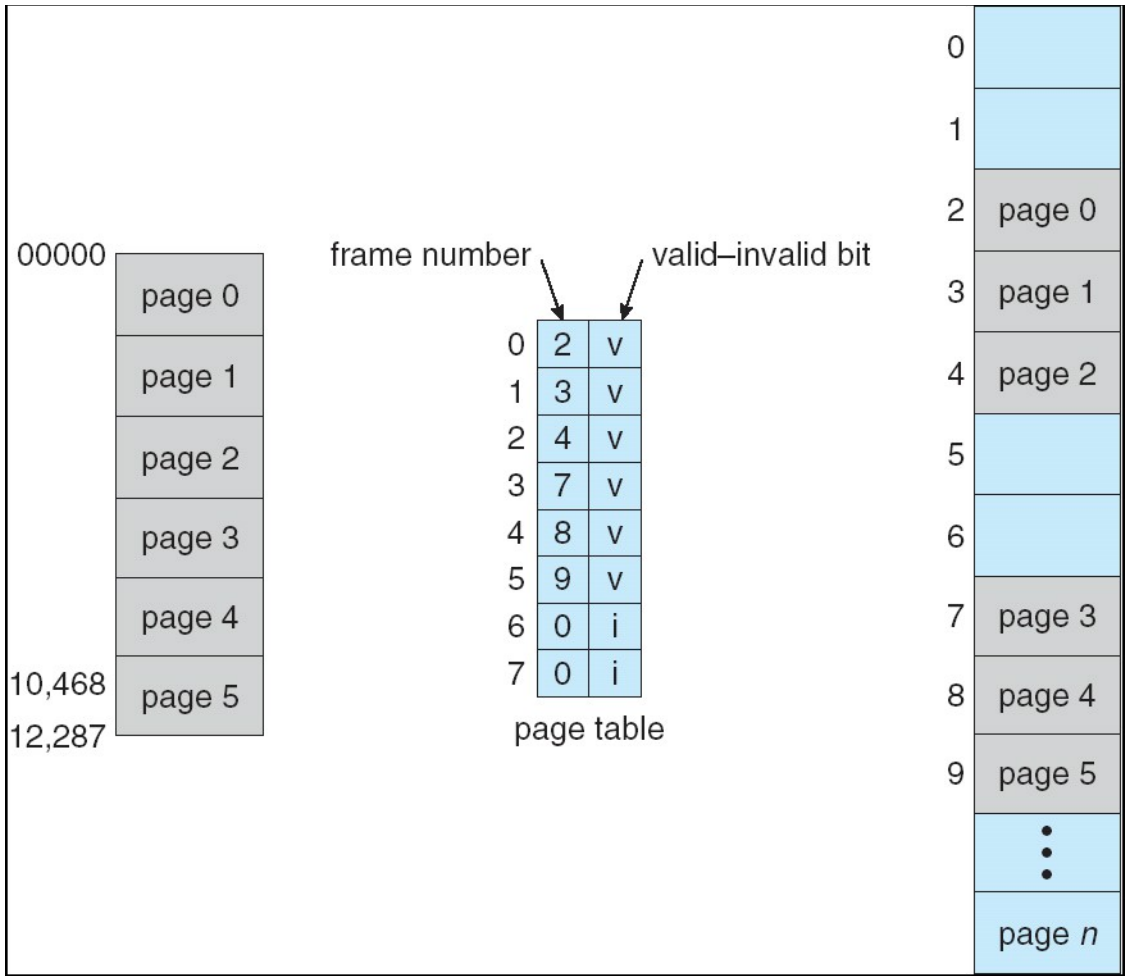


Page table with TLB

- Translation Look-aside Buffer (TLB)
  - associative memory

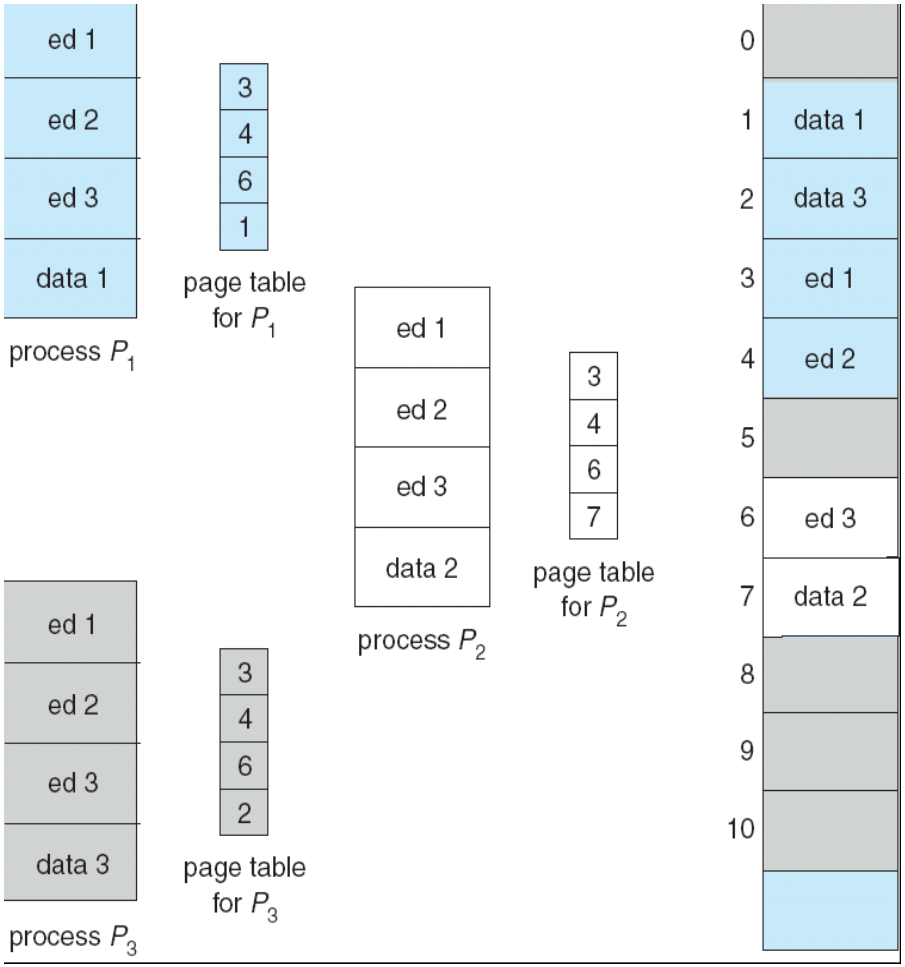


Page table: valid bit



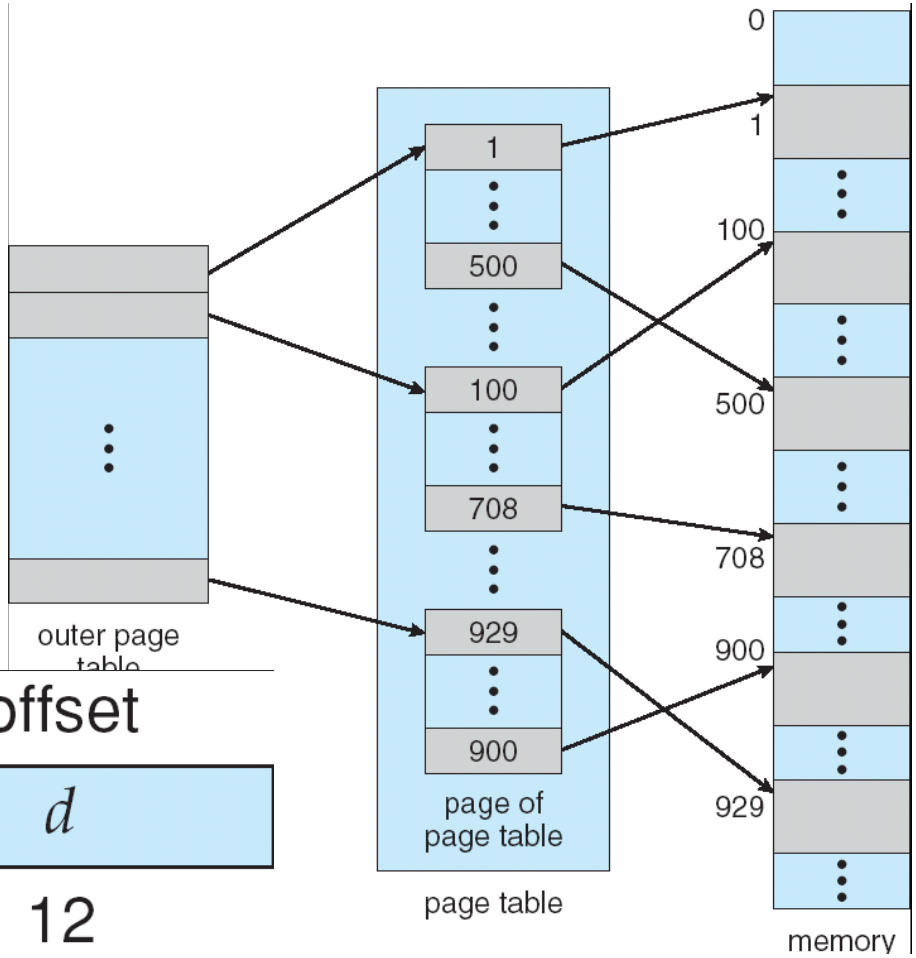
Shared pages

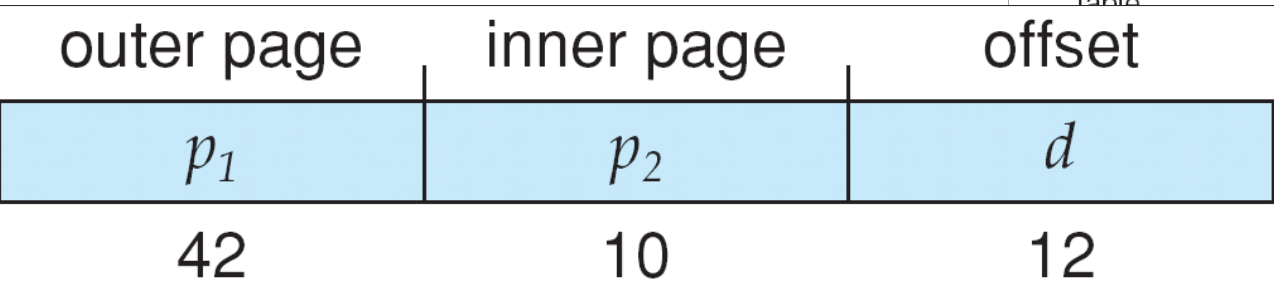
- Shared code
  - one read-only code
  - same address in logical space
- Private code + data
  - one copy per process



Hierarchical page table

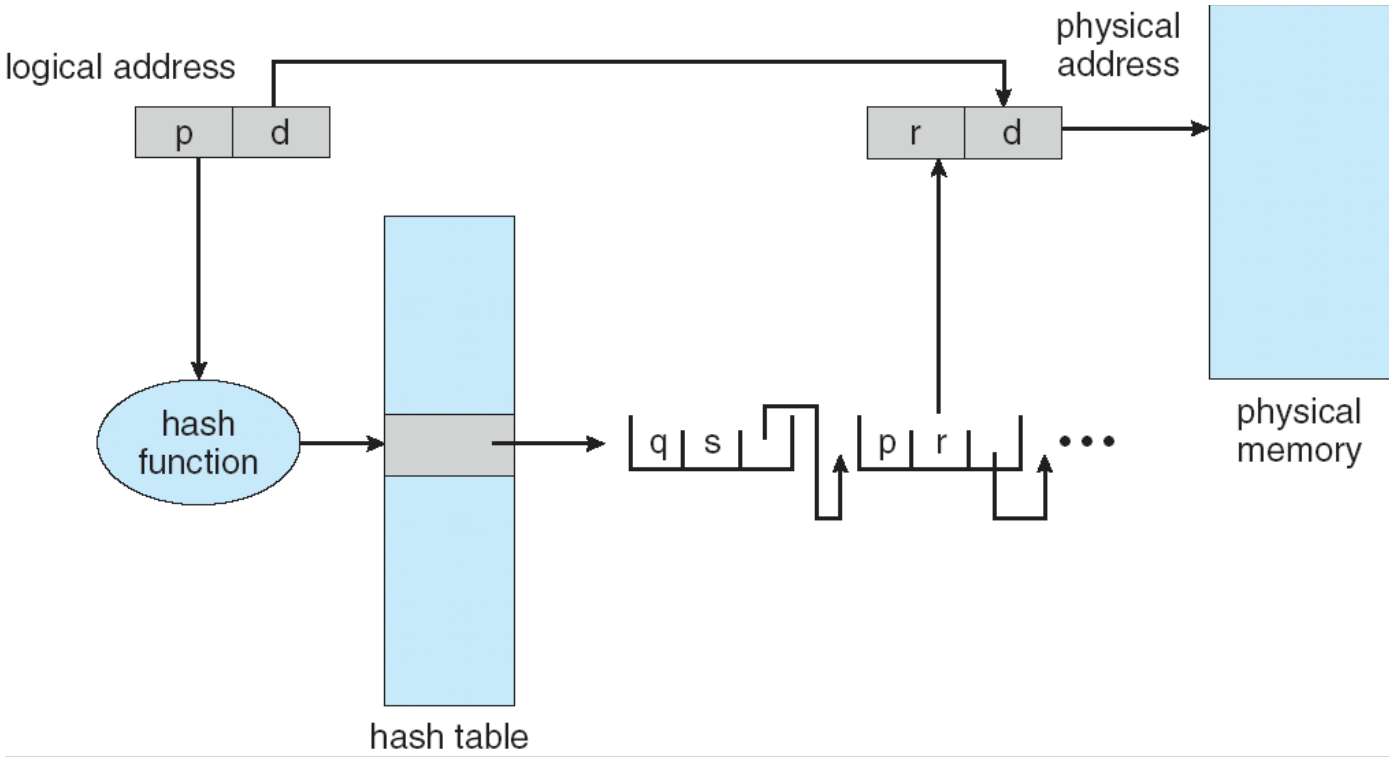
- Difficulty with a table of too many entries
  - where to keep the table
  - how to lookup efficiently
- Solution
  - e.g., 2-level table





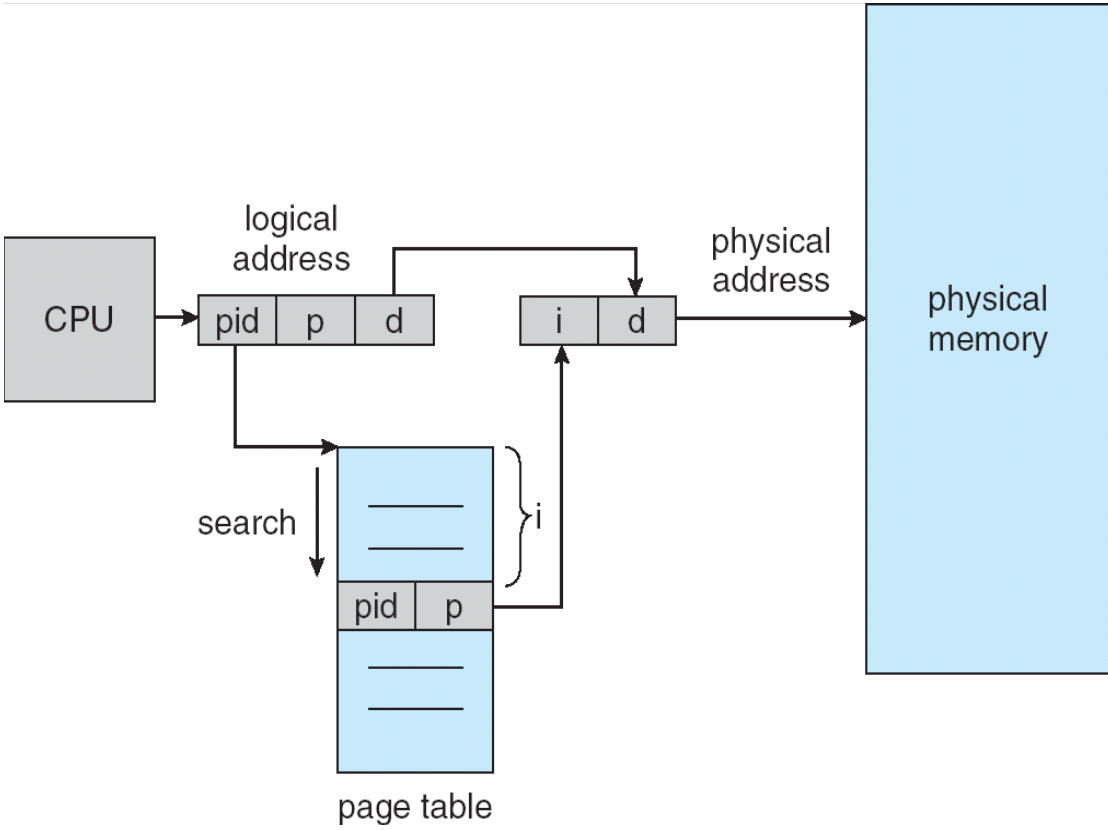
Hash page table

- Hash + linked list



Inverted page table

- When
  - physical space << logical space
- Tradeoff
  - time
  - space



This lecture

- Page table
  - protection
  - shared pages
  - hierarchical, hash, inverted
- Explore further
  - Intel Pentium (OSC7Ch8.7)
  - practice on the chapter-end exercises

Next lecture

- Segmentation and paging
  - read OSC7Ch8